

Section II - Remarks

In a second, non-final Office Action, the examiner rejected claims 1-5, 9-20, and 23-28 under 35 U.S.C. § 103 as being unpatentable over the prior art discussed in the background section of the subject application in view of U.S. Patent No. 6,097,066 to Lee et al. (newly cited). Claims 6-8 were rejected under 35 U.S.C. § 103 as being unpatentable over the former combination of references further in view of Okabe (previously cited). Finally, claims 21-22 were rejected under 35 U.S.C. § 103 as being unpatentable over the prior art discussed in the background section of the subject application in view of Lee et al. and further in view of Corbett et al. (previously cited).

In response, applicants have canceled claim 25, and amended claims 1, 3-5, 7, 8, 10, 12, 14, 23, and 26. Claims 1-24, and 26-28 remain pending for consideration.

Applicants respectfully traverse the obviousness rejection of the pending claims over the prior art discussed in the background section of the subject application in view of Lee et al. According to the Office Action, Figure 6 in Lee et al discloses "a conductive region 550B disposed in the first doped region 500A." However, these identified regions do not suggest or disclose the any aspect of the claimed invention.

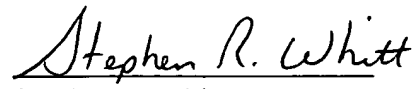
As recited in amended, independent claim 1, the subject invention comprises in combination, "a first doped region of first conductivity type disposed in a semiconductor substrate of second conductivity type, underlying and surrounding the conductive pad; [and] a conductive region of first conductivity type disposed in the first doped region." This description is consistent with the examples set forth in the specification. Moreover, the benefits of this particular relationship between the conductive region and the first doped region is set forth in the specification. (See, for example, the specification at page 15, second paragraph).

In contrast, the regions identified in Lee et al., include a P+ type region 550B formed directly in a P-type semiconductor substrate 500A. The resent invention is clearly distinguished from this structure.

Independent claims 12 and 23 have been similarly amended. Accordingly pending claims 1-24, and 26-28 are allowable over the art of record.

Respectfully submitted,

Date: January 22, 2002

A handwritten signature in cursive script that reads "Stephen R. Whitt". The signature is written in dark ink and is positioned above the printed name and contact information.

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703-433-9208

Section III - Version with markings to show changes

The Claims

Please cancel claim 25, and amend the following claims as shown.

1. (Amended) An integrated circuit device comprising:
 - a conductive pad to receive an input signal from an external signal line;
 - a first doped region of first conductivity type disposed in a semiconductor substrate of second conductivity type, underlying and surrounding the conductive pad;
 - a conductive region of first conductivity type disposed in the first doped region;
 - a first tap region spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage;
 - an output driver transistor having a drain region and a source region, wherein the drain region is electrically coupled to the conductive pad; and
 - a second tap region surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage and the source region.
3. (Amended) The integrated circuit device of claim 2 wherein the first tap region [substantially] completely surrounds the first doped region.
4. (Amended) The integrated circuit device of claim [3] 1 wherein the first tap region is a discontinuous region.
5. (Amended) The integrated circuit device of claim 1 wherein the doping concentration of the first doped region is [of a first doping density of a first conductivity type,] less than the doping concentration of the conductive region [is of a second doping density of the first conductivity type wherein the first doping density is less than the second doping density].
7. (Amended) The integrated circuit device of claim [1] 6 wherein the third doped region is of an opposite conductivity type than the first doped region.

8. (Amended) The integrated circuit device of claim [1] 6 wherein the fourth doped region is a P type doped region and the output driver transistor is an NMOS type transistor.

10. (Amended) The integrated circuit device of claim [1] 5 wherein the first tap region substantially surrounds the first doped region.

12. (Amended) A bond pad for an integrated circuit device, the bond pad comprising:
a conductive bonding layer;
a first doped region of first conductivity type formed in a semiconductor substrate of second conductivity type, underlying and surrounding the conductive bonding layer;
a conductive region of first conductivity type disposed in the first doped region, the conductive region having a surface area at least substantially equal to the surface area of the conductive bonding layer; and
a conductive tap region spaced apart from and surrounding at least a portion of the first doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

14. (Amended) The bond pad of claim 12 wherein the doping concentration of the first doped region is [of a first doping density of a first conductivity type] less than the doping concentration of the conductive region [is of a second doping density of the first conductivity type wherein the first doping density is less than the second doping density].

23. (Amended) A transistor layout for an integrated circuit device having a bond pad, the transistor layout comprising:
a drain region of first conductivity type formed in a semiconductor substrate of second conductivity type, the drain region being electrically coupled to the bond pad;
a source region of second conductivity type; and
a conductive tap region spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage and electrically and physically

coupled to the source region.

26. (Amended) The transistor layout of claim 23 wherein the conductive tap region is spaced proximal to and completely surrounds the drain region.